FIG. 1

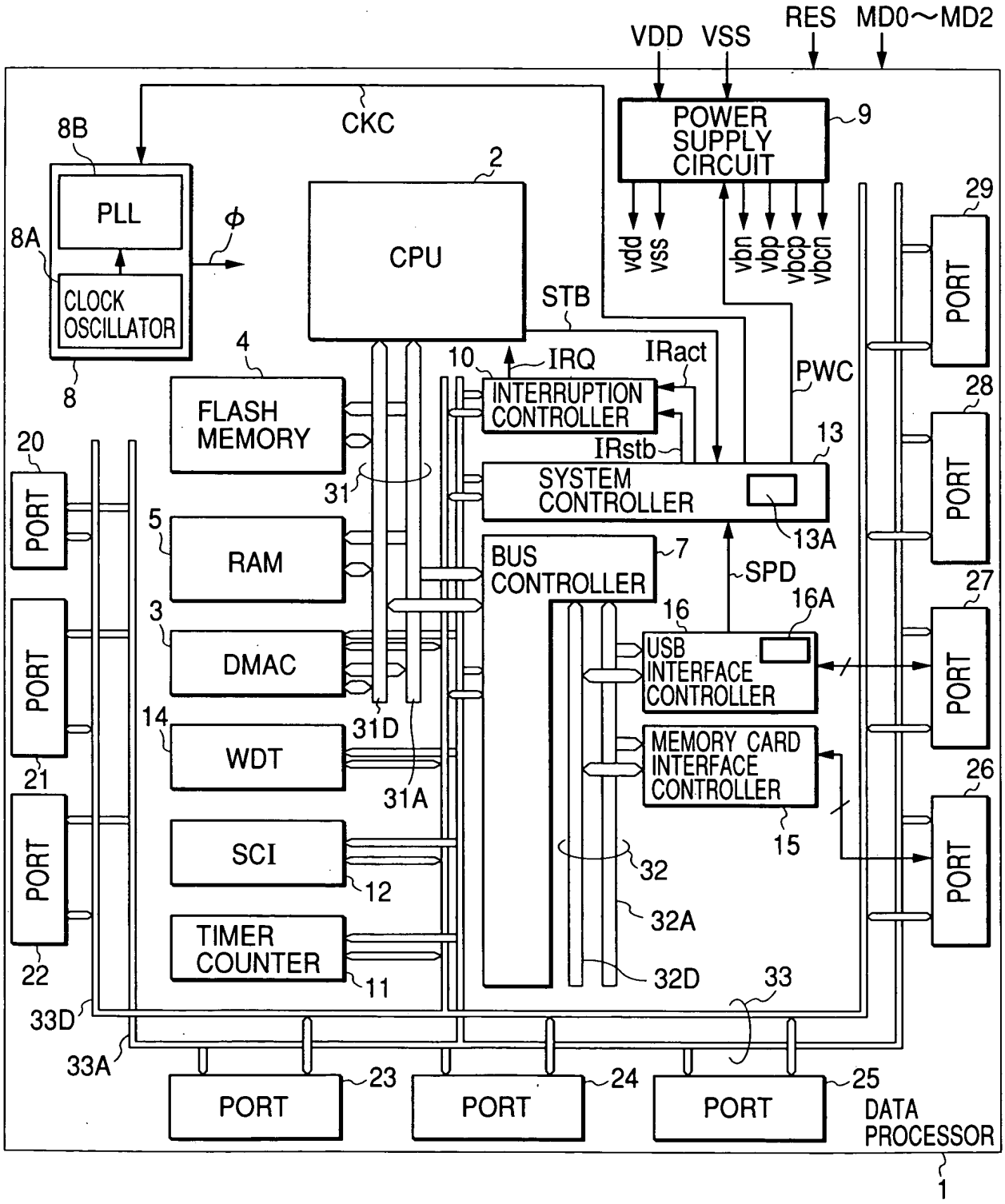

VDD
VSS
RES
MD0~MD2
CKC
8B
PLL
8A
CLOCK OSCILLATOR
8
φ
2
CPU
POWER SUPPLY CIRCUIT
9
vdd
vss
vbn
vbp
vbcp
vbcn
29
PORT
STB
IRact
IRQ
10
INTERRUPTION CONTROLLER
PWC
28
PORT
4
FLASH MEMORY
31
IRstb
13
SYSTEM CONTROLLER
13A
20
PORT
5
RAM
BUS CONTROLLER
7
SPD
16A
27
PORT
3
DMAC
16
USB INTERFACE CONTROLLER
14
WDT
31D
31A
MEMORY CARD INTERFACE CONTROLLER
15
26
PORT
21
PORT
SCI
12
32
32A
22
PORT
TIMER COUNTER
11
32D
33
33D
33A
23
PORT
24
PORT
25
PORT
DATA PROCESSOR
1

FIG. 2

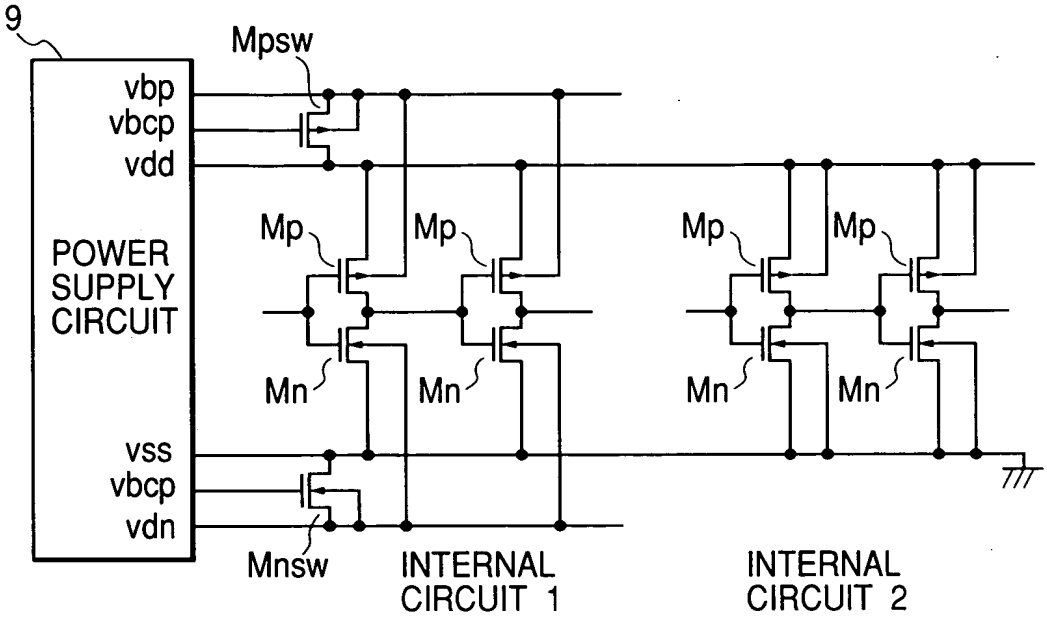

9
Mpsw
vbp
vbcp
vdd
POWER SUPPLY CIRCUIT
Mp
Mn
vss
vbcp
vdn
Mnsw
INTERNAL CIRCUIT 1
INTERNAL CIRCUIT 2

FIG. 3

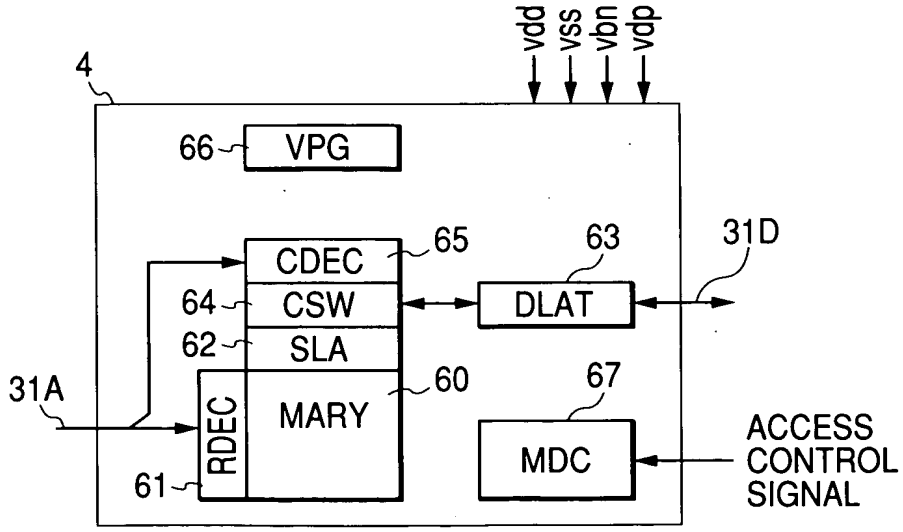

vdd
vss
vbn
vdp
4
66
VPG
CDEC
65
63
31D
64
CSW
DLAT
62
SLA
31A
RDEC
MARY
60
67
61
MDC
ACCESS CONTROL SIGNAL

FIG. 4

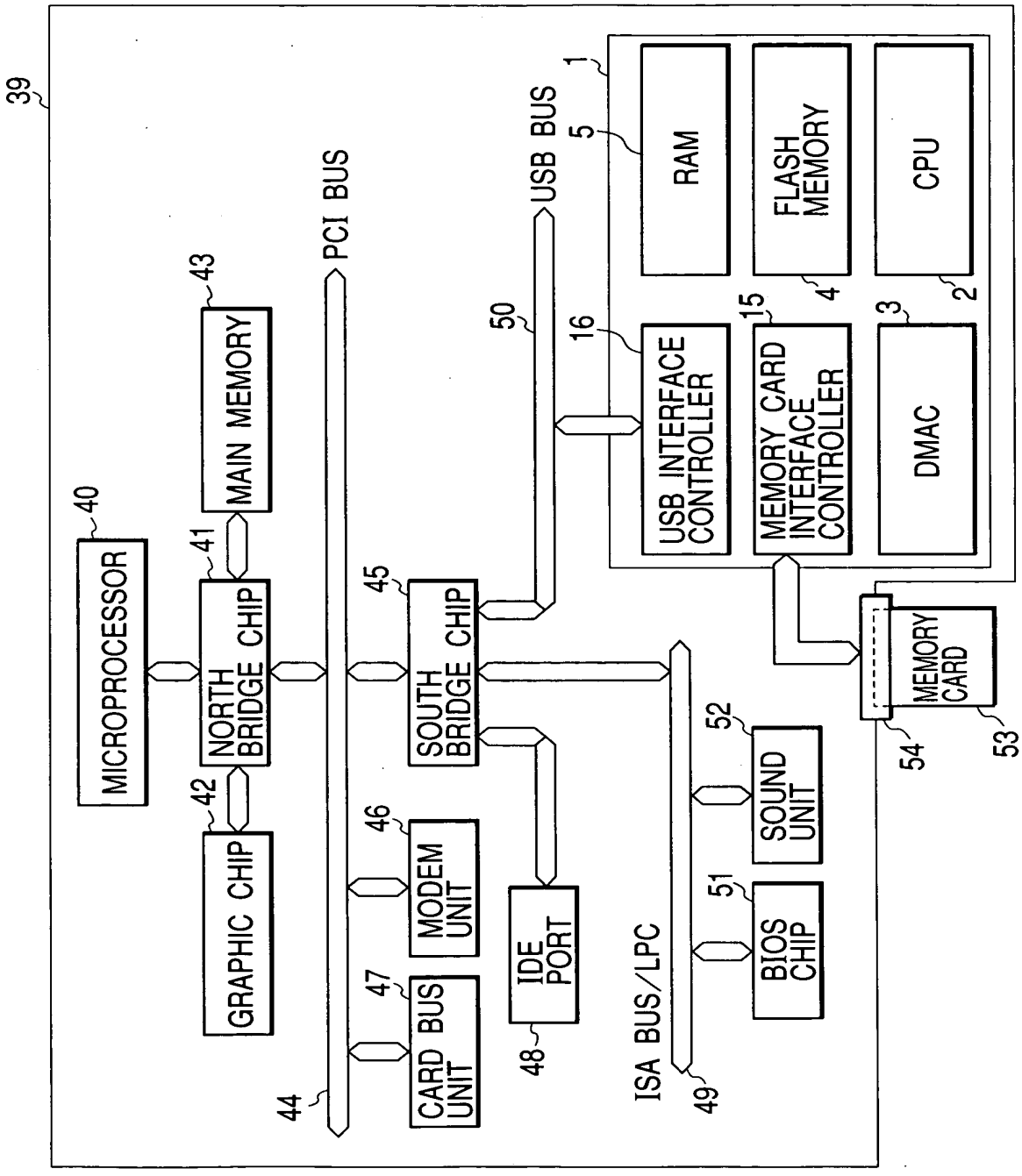

39
MICROPROCESSOR
40
NORTH BRIDGE CHIP
41
MAIN MEMORY
43
GRAPHIC CHIP
42
PCI BUS
44
SOUTH BRIDGE CHIP
45
USB BUS
50
1
RAM
5
FLASH MEMORY
4
CPU
2
USB INTERFACE CONTROLLER
16
MEMORY CARD INTERFACE CONTROLLER
15
DMAC
3
MODEM UNIT
46
CARD BUS UNIT
47
IDE PORT
48
ISA BUS/LPC
49
SOUND UNIT
52
BIOS CHIP
51
MEMORY CARD
53
54

FIG. 5

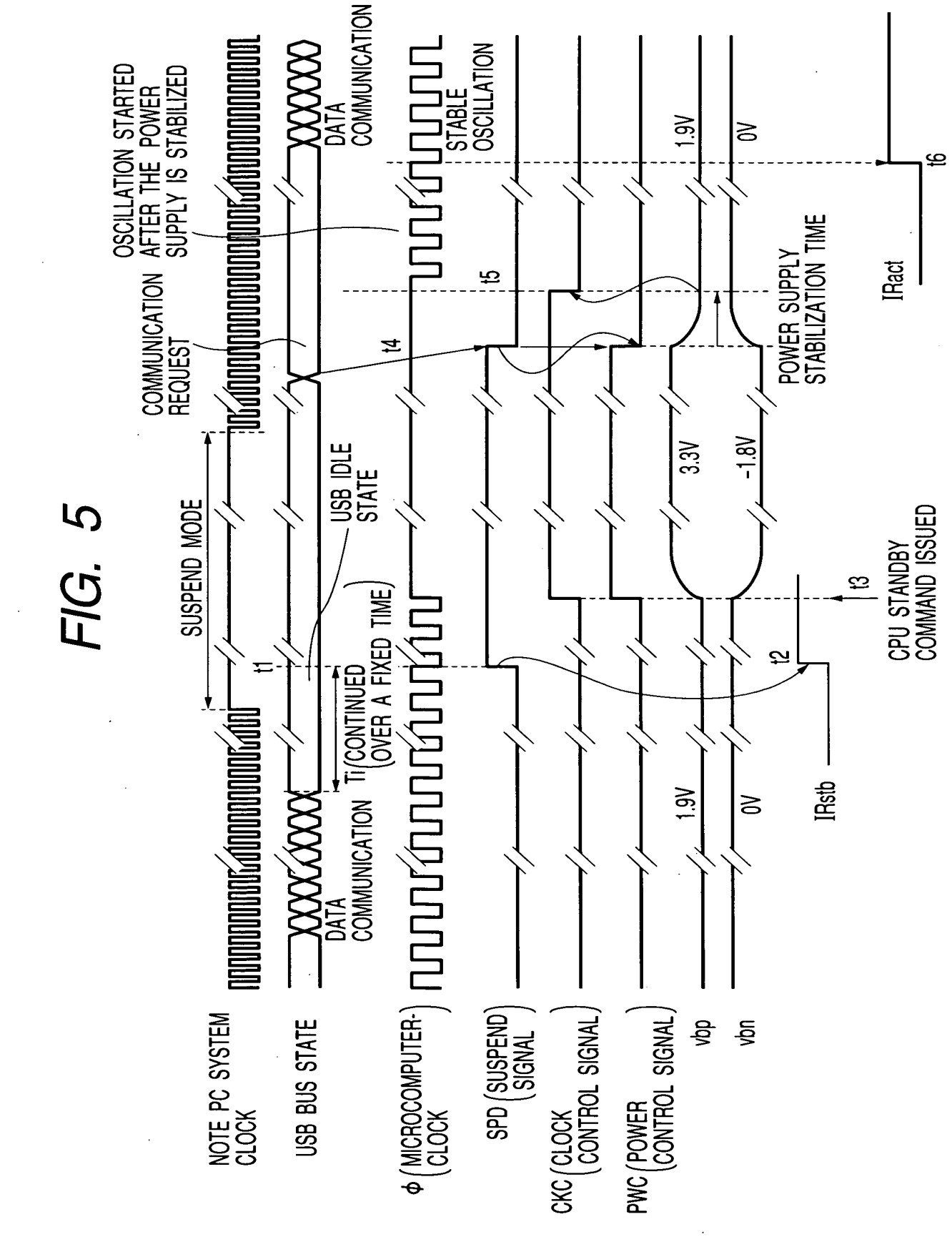

NOTE PC SYSTEM CLOCK
USB BUS STATE
Φ (MICROCOMPUTER-CLOCK)
SPD (SUSPEND SIGNAL)
CKC (CLOCK CONTROL SIGNAL)
PWC (POWER CONTROL SIGNAL)
vbp
vbn
SUSPEND MODE
DATA COMMUNICATION
USB IDLE STATE
Ti (CONTINUED OVER A FIXED TIME)
DATA COMMUNICATION
COMMUNICATION REQUEST
OSCILLATION STARTED AFTER THE POWER SUPPLY IS STABILIZED
STABLE OSCILLATION
t1
t2
t3
t4
t5
t6
1.9V
0V
3.3V
-1.8V
1.9V
0V
IRstb
IRact
POWER SUPPLY STABILIZATION TIME
CPU STANDBY COMMAND ISSUED

FIG. 6

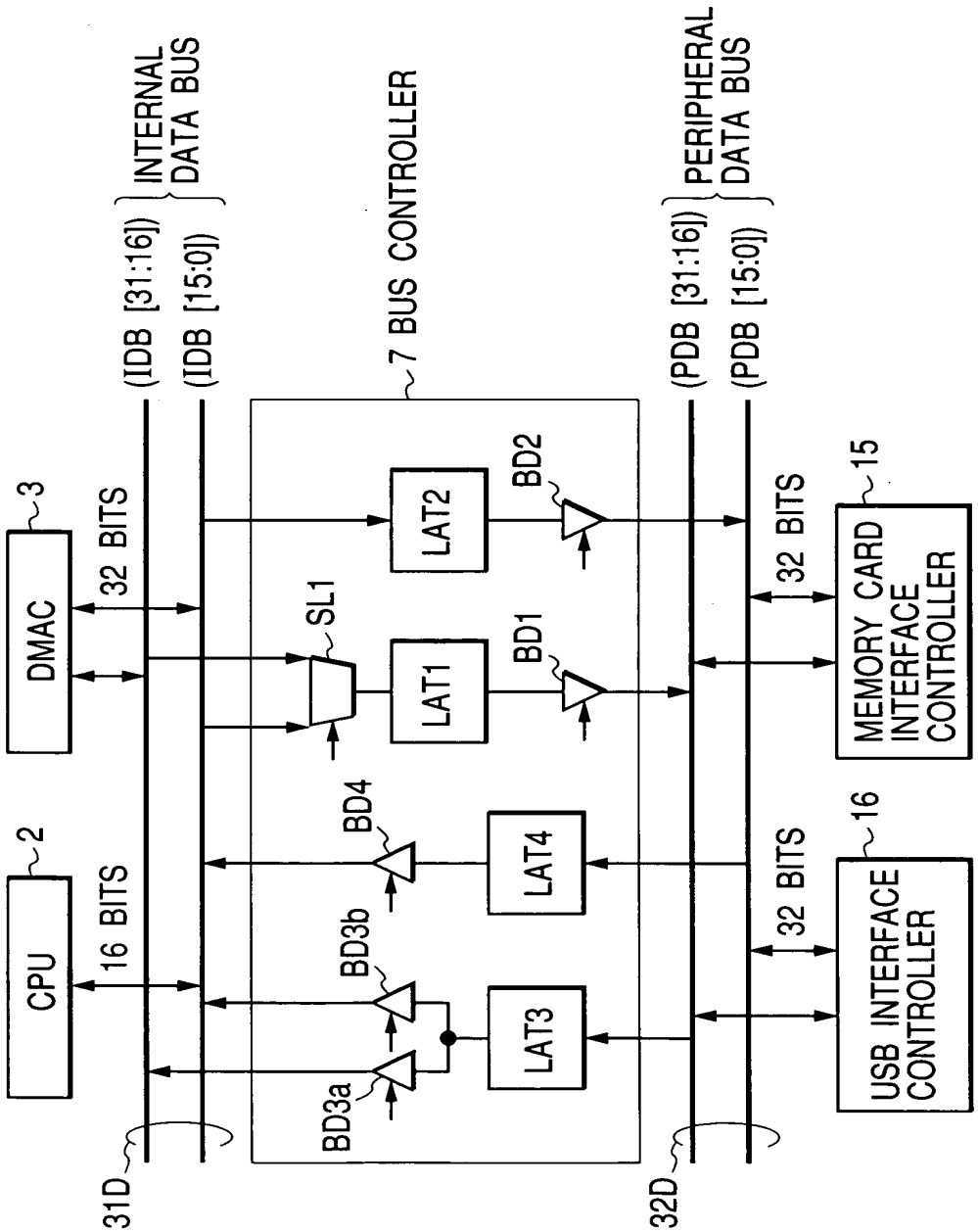

CPU
2
16 BITS
DMAC
3
32 BITS
(IDB [31:16])
(IDB [15:0])
INTERNAL DATA BUS
7 BUS CONTROLLER
SL1
LAT1
LAT2
LAT3
LAT4
BD1
BD2
BD3a
BD3b
BD4
31D
32D
(PDB [31:16])
(PDB [15:0])
PERIPHERAL DATA BUS
32 BITS
32 BITS
32 BITS
MEMORY CARD INTERFACE CONTROLLER
15
USB INTERFACE CONTROLLER
16

FIG. 7

31
23
15
7
0
D3
D2
D1
D0
LONG-WORD DATA :
LOWER 2 BITS OF ADDRESS :
00
01
10
11

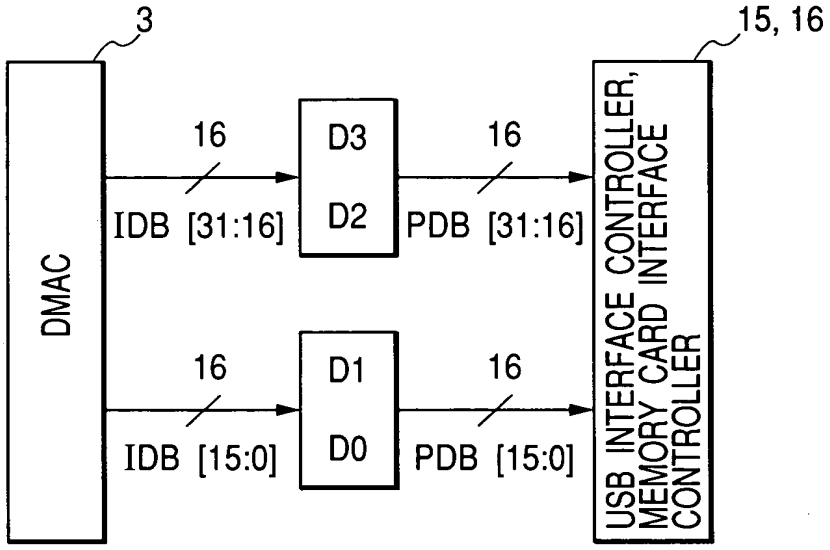
FIG. 8

	ADDRESS	DATA				CPU	DMAC
	1, 0	31	23	15	7..0		
LONG-WORD	xx	D3	D2	D1	D0	×	○
WORD	0x	–	–	D3	D2	○	○
	1x	–	–	D1	D0	○	○
BYTE	00	–	–	D3	–	○	○
	01	–	–	–	D2	○	○
	10	–	–	D1	–	○	○
	11	–	–	–	D0	○	○

FIG. 9

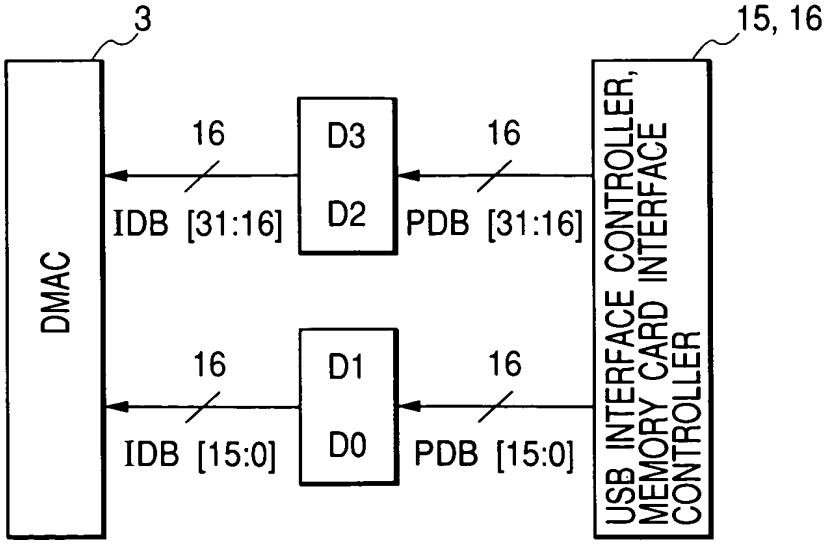
	ADDRESS	DATA			
	1, 0	31	23	15	7..0
LONG-WORD	xx	D3	D2	D1	D0
WORD	0x	D3	D2	–	–
	1x	–	–	D1	D0
BYTE	00	D3	–	–	–
	01	–	D2	–	–
	10	–	–	D1	–
	11	–	–	–	D0

FIG. 10



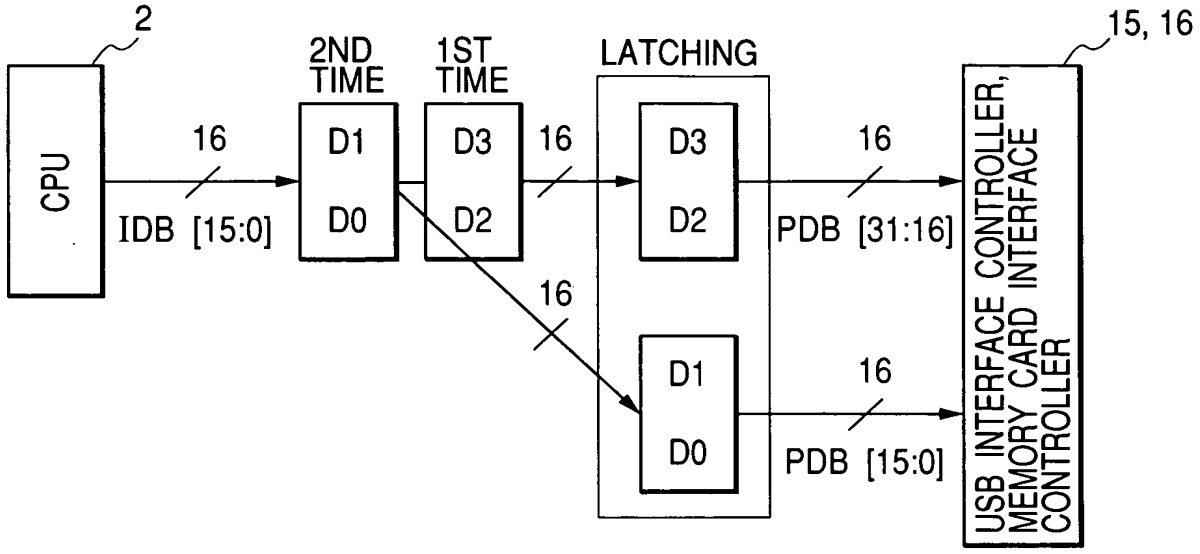
(DMAC LONG-WORD WRITING)

FIG. 11



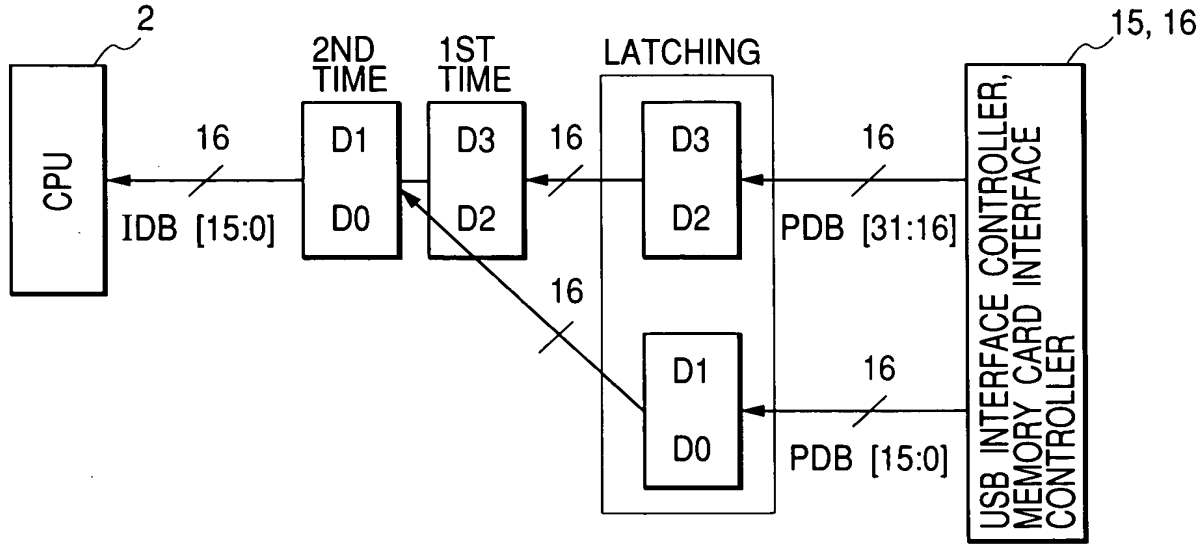
(DMAC LONG-WORD READING)

FIG. 12



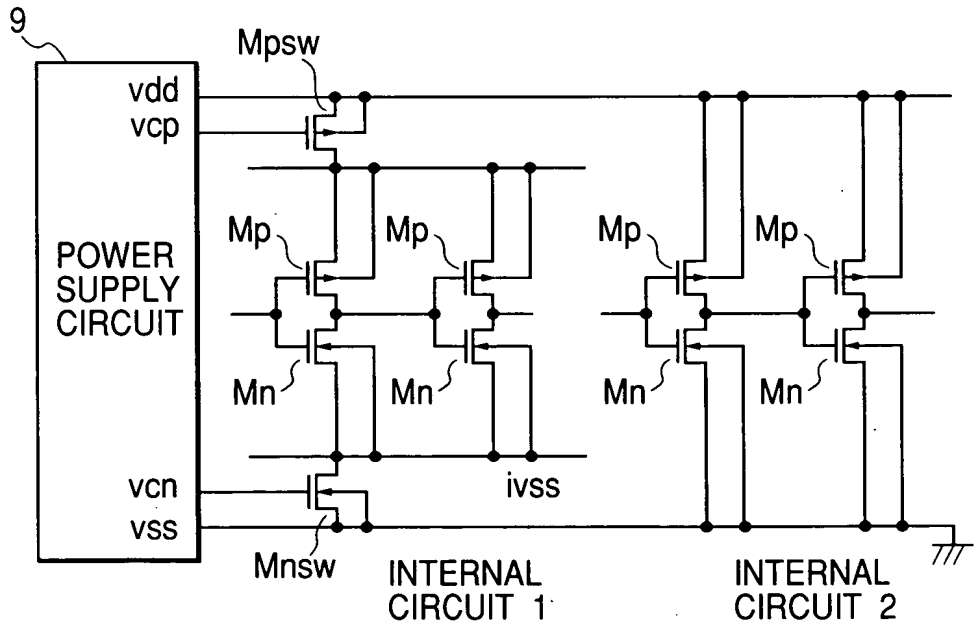
(CPU LONG-WORD WRITING)

FIG. 13



(CPU LONG-WORD READING)

FIG. 14


9
Mpsw
vdd
vcp
POWER
SUPPLY
CIRCUIT
Mp
Mp
Mp
Mp
Mn
Mn
Mn
Mn
ivss
vcn
vss
Mnsw
INTERNAL
CIRCUIT 1
INTERNAL
CIRCUIT 2